

PHASE 1: FIND THE SLOT BOUNDARY

CORRELATE THE RECEIVED SIGNAL WITH THE PRIMARY SYNCHRONIZATION CODE OVER A RANGE OF DELAY VALUES FOR EACH OF A NUMBER OF RECEIVED SLOTS

101

FOR EACH TESTED DELAY LOCATION, ACCUMULATE THE CORRELATED VALUES OBTAINED FROM THE RECEIVED SLOTS

102

EXTRACT THE DELAY CORRESPONDING TO THE LARGEST ACCUMULATED PEAK. THIS IS THE SLOT BOUNDARY.

103

PHASE 2:
FIND THE FRAME BOUNDARY

CORRELATE THE RECEIVED SIGNAL WITH THE SECONDARY SYNCHRONIZATION CODE, USING THE DELAY FOUND IN STEP 103

104

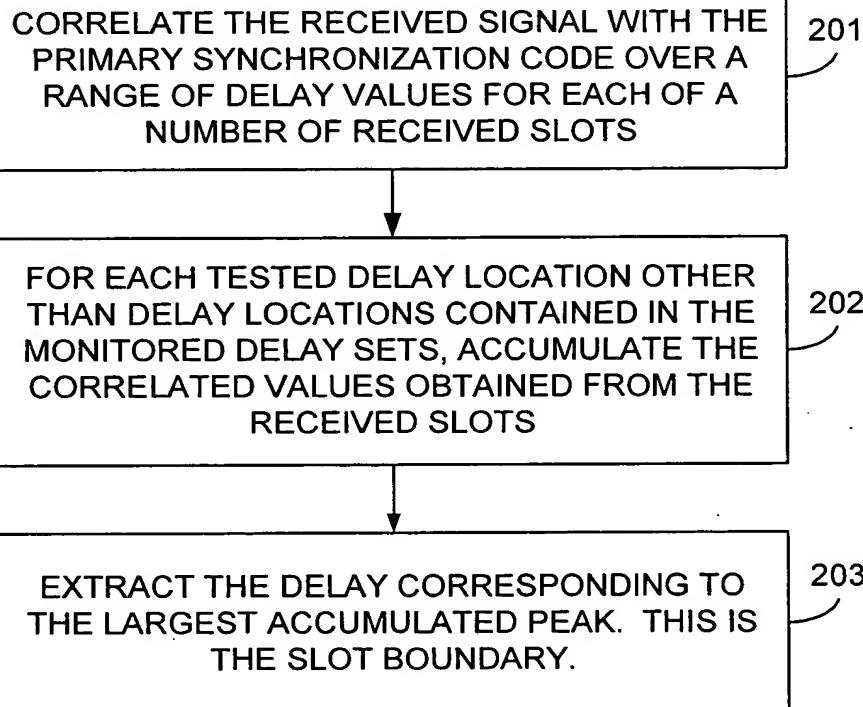
PHASE 3: FIND THE SCRAMBLING
CODE FOR THE CELL

USING KNOWN OFFSET FROM FRAME BOUNDARY, CORRELATE KNOWN SCRAMBLING CODES AGAINST RECEIVED SCRAMBLING CODE TO FIND BEST CORRELATION

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**FIG. 1
(PRIOR ART)**

PHASE 1: FIND THE SLOT BOUNDARY



PHASE 2:
FIND THE FRAME BOUNDARY



PHASE 3: FIND THE SCRAMBLING
CODE FOR THE CELL

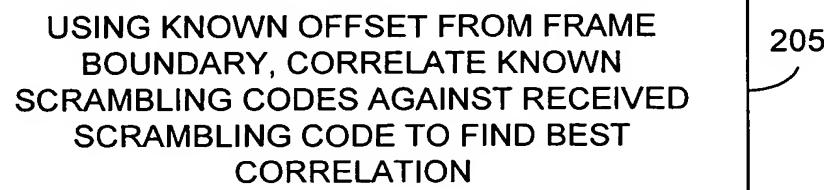


FIG. 2

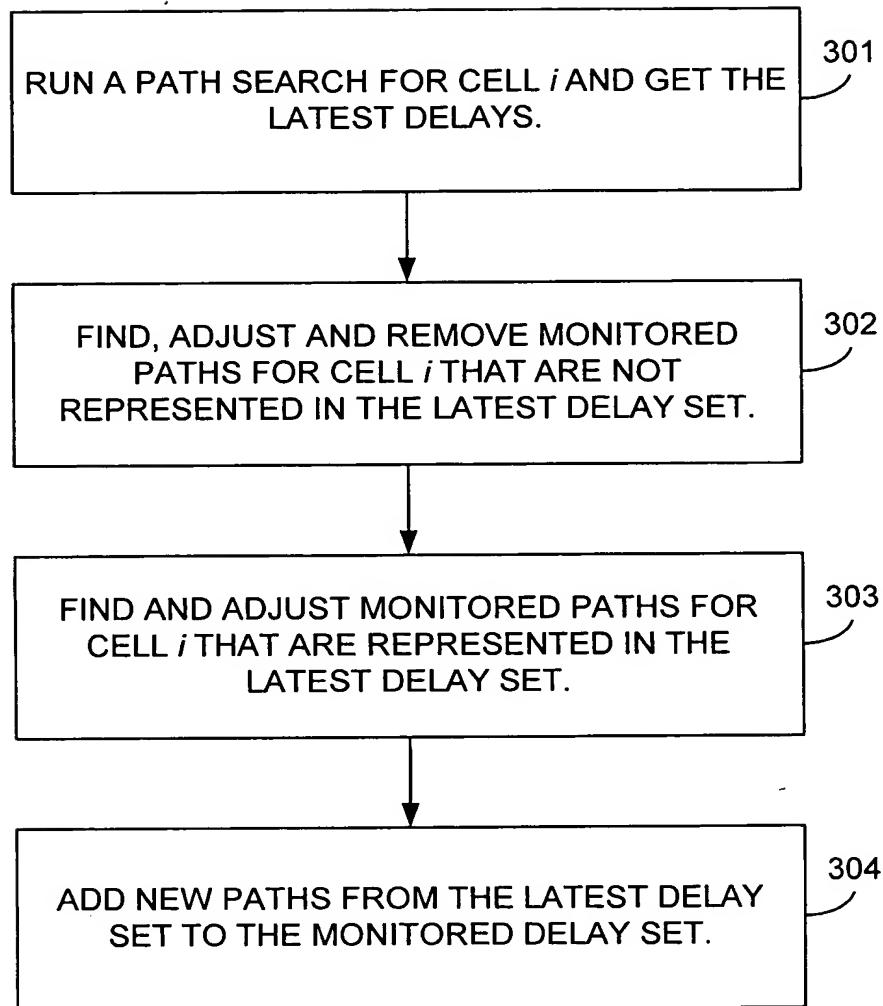


FIG. 3

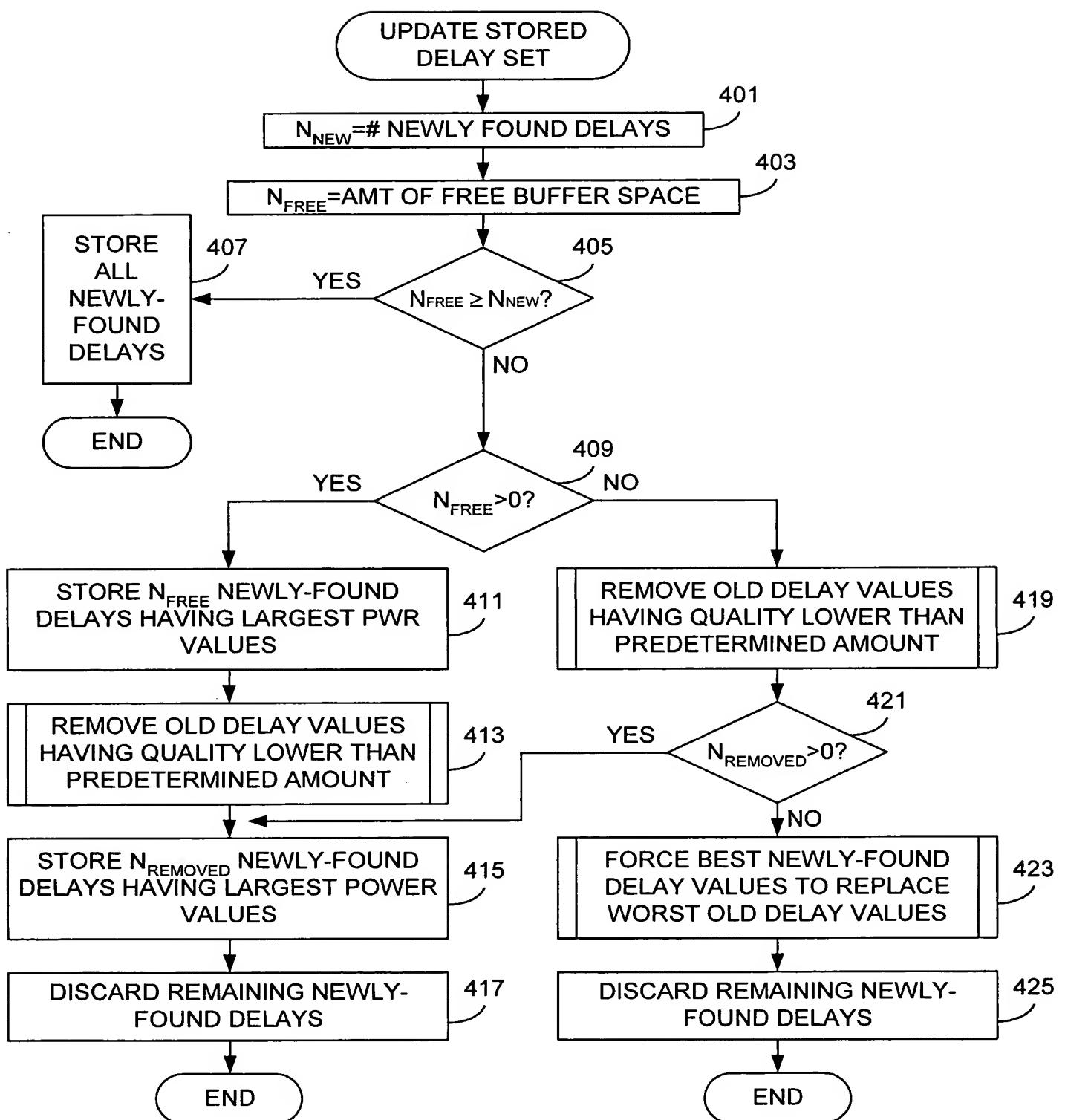


FIG. 4A

413, 419

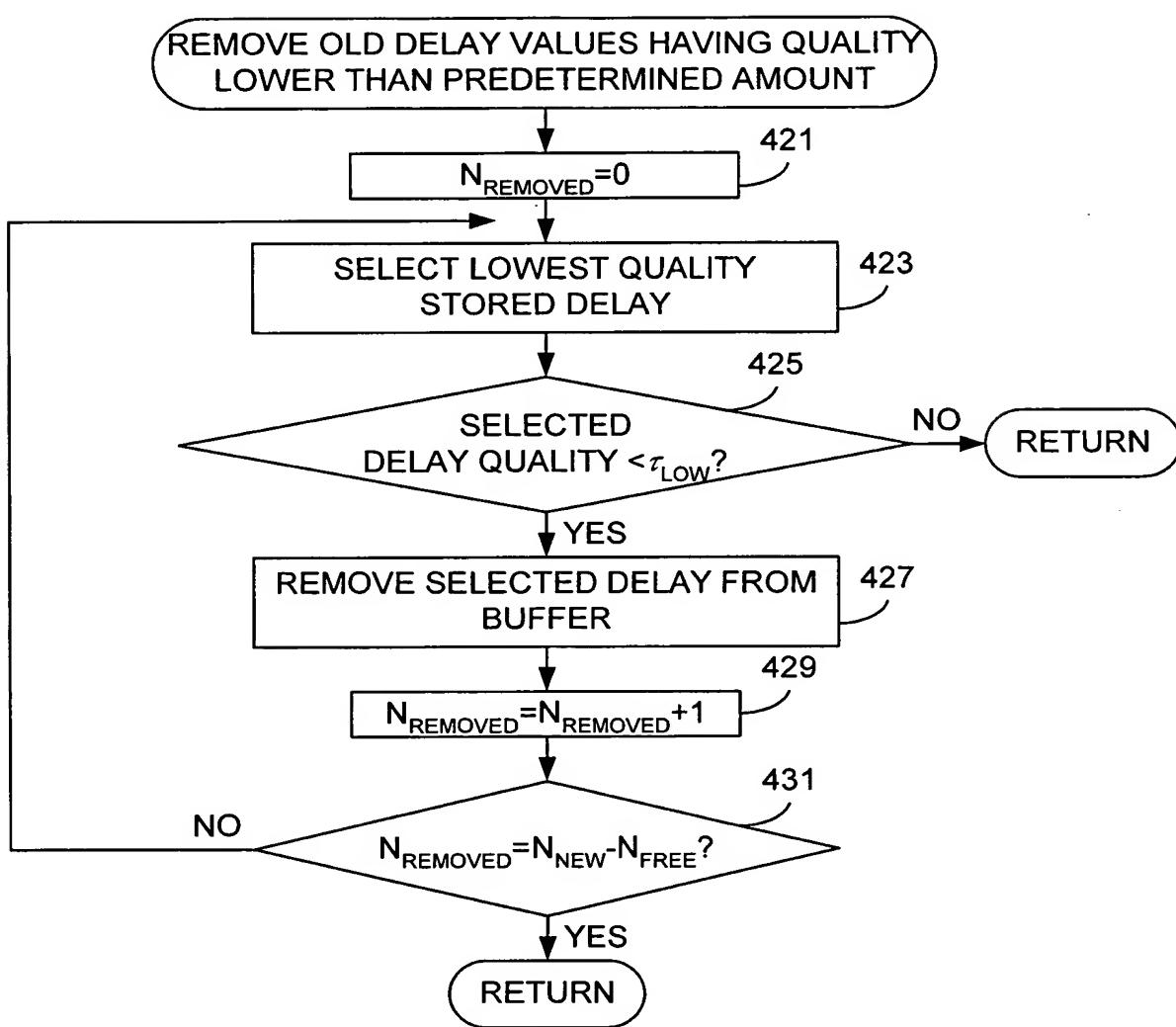


FIG. 4B

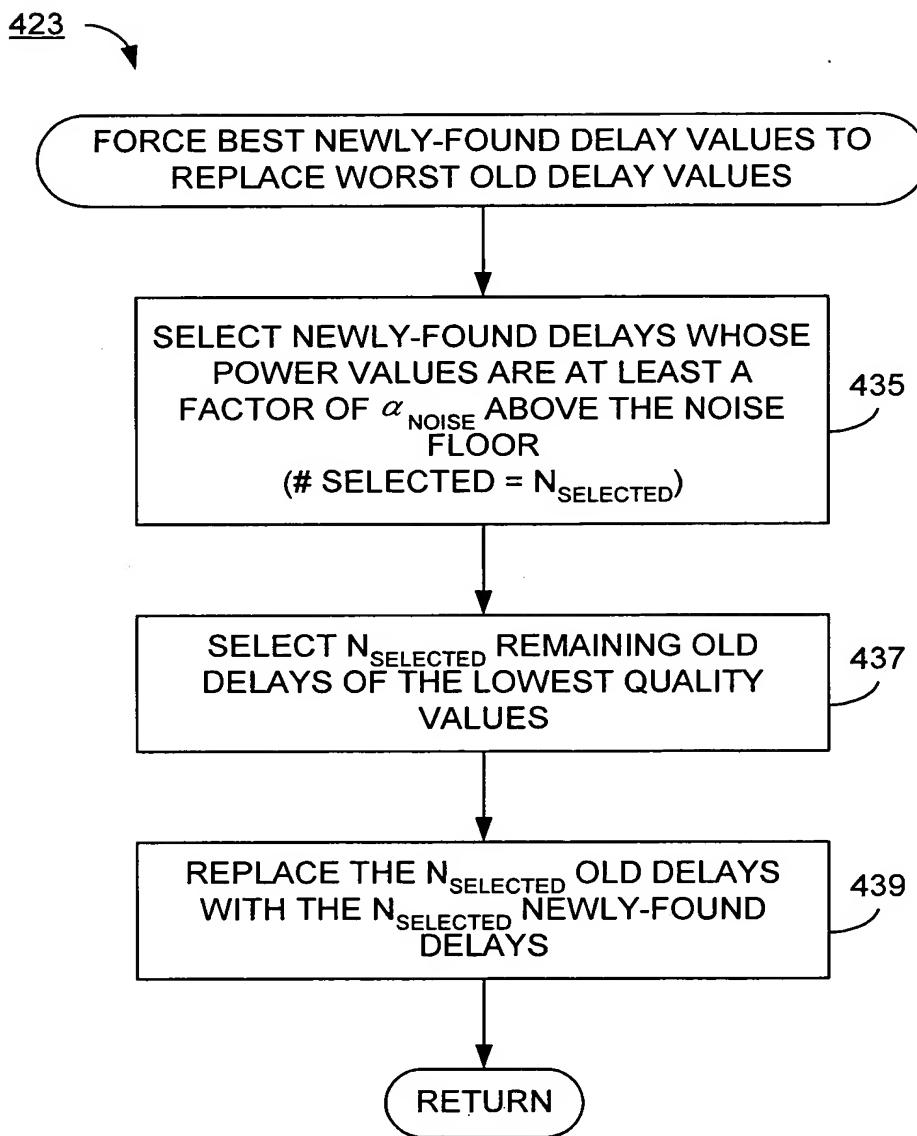


FIG. 4C